BK7256 Datasheet

DS-BK7256-E02 V1.0

2022/11/21

Contents

1. Features

Wi-Fi

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20/40 MHz channel bandwidth for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports uplink Orthogonal Frequency Division Multiple Access (UL OFDMA)
- Supports individual Target Wake Time (iTWT)
- TX and RX low-density parity check (LDPC) support for extended range
- WPA/WPA2/WPA3-Personal support for enhanced security
- Working mode: STA, AP, Direct
- Concurrent AP + STA
- Integrated Bluetooth/WLAN coexistence (PTA)
- TX power up to +18 dBm
- RX sensitivity -99 dBm

Bluetooth

- Dual-mode Bluetooth 5.2 compliant
- Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2 Mbps and 3 Mbps, Low Energy (LE) 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Advertising extensions
- Bluetooth direction finding: Angle of Arrival (AoA) and Angle of Departure (AoD)
- Supports an antenna array with up to sixteen antennae for precise indoor positioning

Core and Memory

- Dual 32-bit RISC-V MCUs at up to 320 MHz:
  - Each core features a double-precision floating point unit (FPU)
  - Each core has 32 K ITCM + 32K DTCM + 64K ICache + 16K DCache
  - Each core includes a memory protection unit (MPU)
  - Each core supports DSP instructions
- EEMBC CoreMark® score: 1 core at 320 MHz: 3.57 CoreMark/MHz
- SiP Flash: 4 MB or none

- 8 MB SiP PSRAM
- 512 KB Share SRAM
- 64 KB ROM
- 32-byte eFuse
- 8 Kbit OTP
- JTAG/UART for debug and download
- SPI flash download

Security

- Isolated secure element (FIPS 140-2 Level 2 certified) with hardware cryptography
- Secure boot
- Unique ID and secure storage
- Secure update and anti-rollback
- Lifecycle management such as secure debug
- Flash encryption
- Cryptographic hardware acceleration:
  - Crypto accelerator: DES, AES-128/192/256, ChaCha20-128/256, SM4-128
  - Public key accelerator: ECDSA-P256/P384, RSA-2048/3072, SM2
  - Hash: SHA-224/256, SHA-384/512, HMAC, Poly1305, SM3-512
  - True Random Number Generator (TRNG)
- Key derivation function (KDF)

Clock Management

- External oscillator: 26 MHz crystal oscillator (X26M), 32.768 kHz crystal oscillator (X32K)
- Internal oscillator: 32 kHz ring oscillator (ROSC), 26 ~ 240 MHz digitally controlled oscillator (DCO)
- 320/480 MHz PLL (DPLL)
- Audio PLL (APLL)

Power Management

- 2.7 to 5.0 V VBAT supply
- On-chip power-on reset (POR) and brown-out detector (BOD)
- Embedded buck (DC-DC) converter and LDO regulators
- Low power consumption:
  - Active mode RX: 63 mA

- Active mode TX: 250 mA
- Low voltage standby mode: 150 µA
- Deep sleep mode: 15 µA
- Shutdown mode: 2.0 µA

Peripherals

- 48 GPIOs
- 2x SPI
- 1x QSPI
- 3x UART: 1 with hardware flow control, 1 with flash download support
- 1x SD/SDIO
- 2x I2C
- 1x full-speed USB OTG (FS)
- 1x CAN controller with CAN FD
- 1x general-purpose DMA controller (GDMA) with 12 channels
- 1x DMA2D controller
- 1x LCD interface (16-bit parallel RGB and I8080)
- 1x JPEG hardware encoder/decoder
- 1x 8-bit CIS DVP camera interface
- Up to 12x 32-bit PWM channels
- 1x I2S
- 2x audio ADC
- 2x audio DAC
- Four-band digital hardware equalizer
- SBC accelerator
- 13-bit SAR ADC, up to 8 channels
- 2x 32-bit general-purpose timer/counter
- 2x watchdog
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor
- Up to 16x touch sensing IO

Packaging

- QFN80 package, 8 x 8 mm
- QFN68 package, 8 x 8 mm
- Operating temperature range: -40 up to +125 ℃

Applications

- Central control panel
- Home Appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart Plug
- Smart Lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

2. Overview

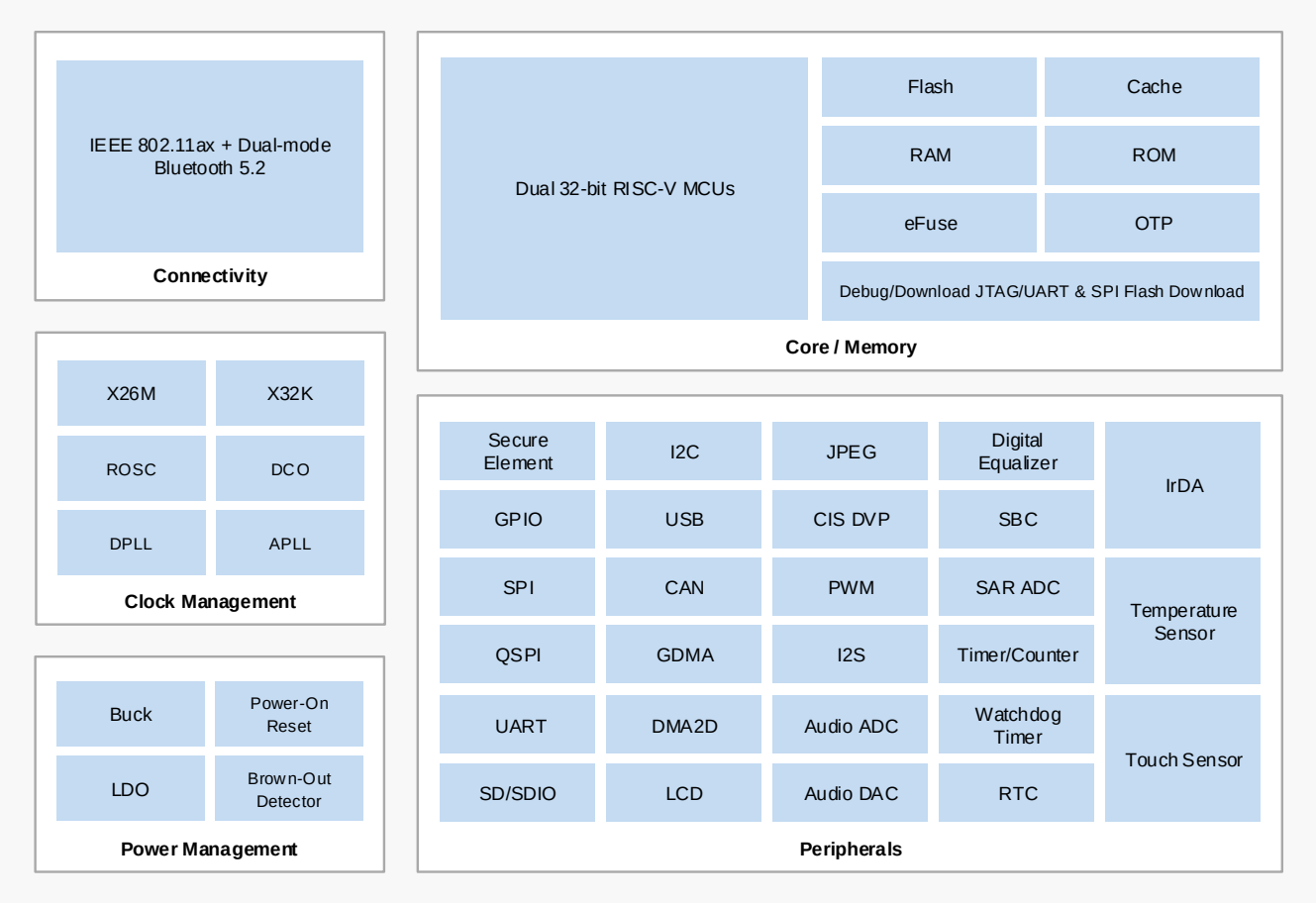
The BK7256 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth 5.2 combo solution designed for applications that require high security and abundant resources. The integration of dual 32-bit RISC-V MCUs and comprehensive set of peripherals makes the BK7256 ideal for advanced Internet of Things (IoT) applications.

The BK7256 provides state-of-the-art security based on a powerful security architecture. It offers an isolated and immutable platform root of trust to provide security services, such as secure boot and cryptographic operations, to applications running on a non-secure processing environment.

Using advanced design techniques and ultra-low-power process technology, the BK7256 delivers high integration and minimal power consumption for central control panels, smart lighting, smart home and other complex IoT applications.

Figure 2-1 shows the general block diagram of BK7256.

Figure 2-1 BK7256 Block Diagram



The BK7256 devices are offered in two packages. The set of included peripherals varies depending on package. Table 2-1 shows the list of peripherals available on each package.

Table 2-1 Device Options and Features

Feature		QFN80	QFN68
Flash		-	4 MB
PSRAM		8 MB	8 MB
GPIO		48	48
SPI	Master/Slave	2	2
QSPI		1	1
UART		3	3
SD/SDIO		1	1
I2C	Master/Slave	2	2
USB OTG		1	1
CAN		1	1
GDMA		1	1
DMA2D		1	1
LCD		1	1
JPEG encoder/decoder		1	1
CIS DVP camera interface		1	1
PWM	PWM0 ~ 11	12	12
I2S	Master/Slave	1	1
Audio ADC		2	1
Audio DAC		Stereo	Mono
Digital equalizer		Yes	Yes
SBC accelerator		Yes	Yes
SAR ADC	13 bits	1	1
	Number of channels	8	8
General-purpose timer/counter		2	2
Watchdog		2	2
Real-time Counter (RTC)		1	1

Feature		QFN80	QFN68
IrDA		1	1
Temperature sensor		1	1
Touch sensing IO	TS0 ~ 15	16	16
Package		8 x 8 mm QFN80	8 x 8 mm QFN68
Operating voltage		2.7 to 5.0 V	
Operating temperature		-40 to +125 ℃	

3. Pin Description

The BK7256 provides WLAN and Bluetooth functionality in two packages ranging from 68 pins to 80 pins.

3.1 QFN80 Pin Description

Figure 3-1 shows the pin assignments of the 8 x 8 mm, 80-pin QFN package..

Figure 3-1 QFN80 Pin Assignments

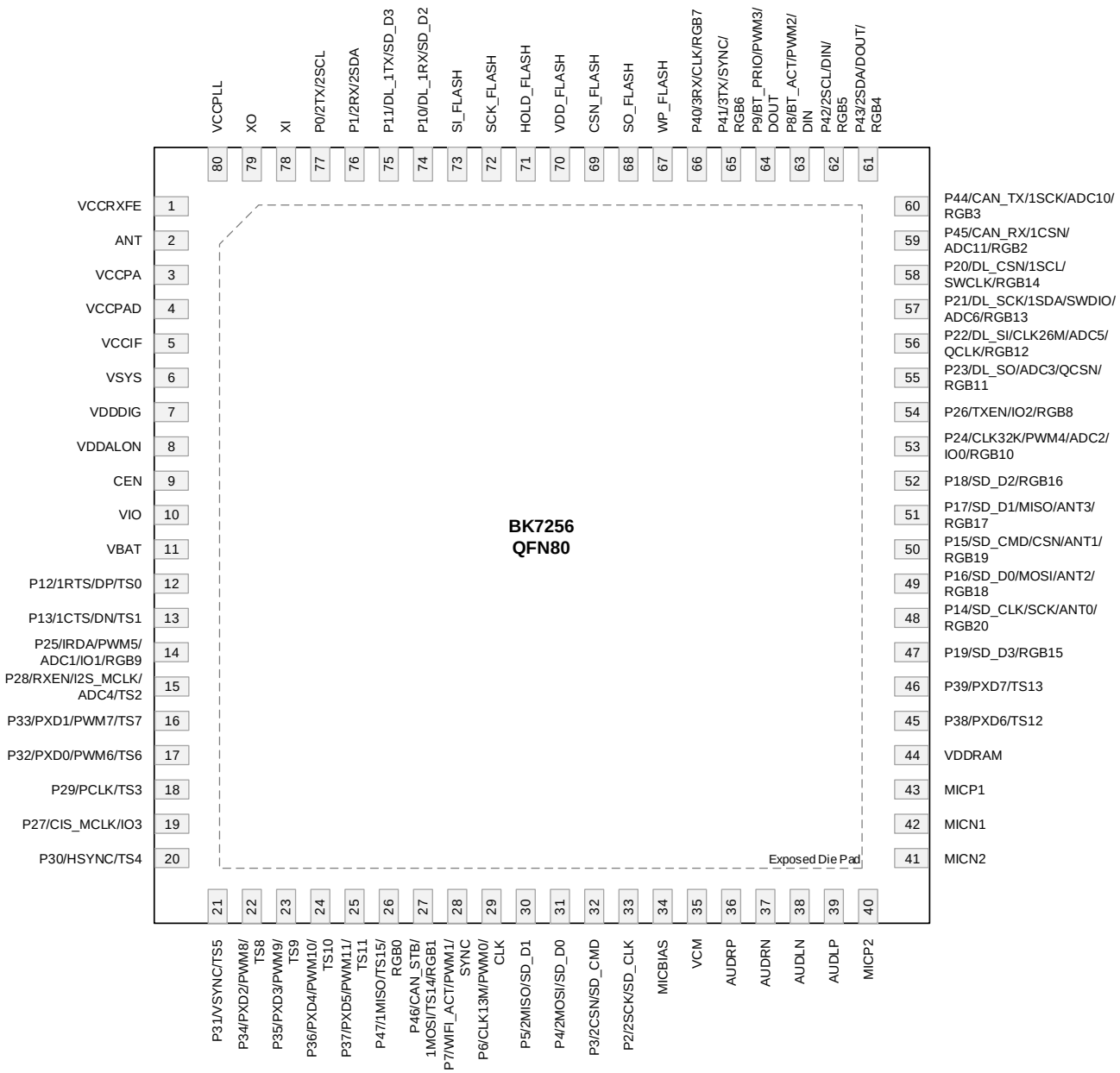


Table 3-1 shows the pin descriptions of the QFN80 package.

Table 3-1 QFN80 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCPAD	-	Analog input	RF PA driver power supply
5	VCCIF	-	Analog input	IF power supply
6	VSYS	-	Analog output	System LDO output
7	VDDDIG	-	Analog output	Digital LDO output
8	VDDALON	-	Analog output	Always-on LDO output
9	CEN	-	Analog input	Chip enable, active high
10	VIO	-	Analog output	IO LDO/BUCK output
11	VBAT	-	Power	Chip power supply
12	P12/1RTS/DP/TS0	I/O	Digital/Analog	• GPIO12 • UART1: RTS • USB: DP • Touch sensor 0
13	P13/1CTS/DN/TS1	I/O	Digital/Analog	• GPIO13 • UART1: CTS • USB: DN • Touch sensor 1
14	P25/IRDA/PWM5/ADC1/IO1/ RGB9	I/O	Digital/Analog	• GPIO25 • IrDA TX/RX • PWM5 (differential with PWM4) • ADC1 • QSPI: IO1 • LCD: RGB9
15	P28/RXEN/I2S_MCLK/ADC4/ TS2	I/O	Digital/Analog	• GPIO28 • RXEN is high when Wi-Fi RF is receiving • I2S: MCLK

Pin #	Name	I/O	Type	Description
				• ADC4 • Touch sensor 2
16	P33/PXD1/PWM7/TS7	I/O	Digital/Analog	• GPIO33 • CIS: PXD1 • PWM7 (differential with PWM6) • Touch sensor 7
17	P32/PXD0/PWM6/TS6	I/O	Digital/Analog	• GPIO32 • CIS: PXD0 • PWM6 (differential with PWM7) • Touch sensor 6
18	P29/PCLK/TS3	I/O	Digital/Analog	• GPIO29 • CIS: PCLK • Touch sensor 3
19	P27/CIS_MCLK/IO3	I/O	Digital/Analog	• GPIO27 • CIS: MCLK • QSPI: IO3
20	P30/HSYNC/TS4	I/O	Digital/Analog	• GPIO30 • CIS: HSYNC • Touch sensor 4
21	P31/VSYNC/TS5	I/O	Digital/Analog	• GPIO31 • CIS: VSYNC • Touch sensor 5
22	P34/PXD2/PWM8/TS8	I/O	Digital/Analog	• GPIO34 • CIS: PXD2 • PWM8 (differential with PWM9) • Touch sensor 8
23	P35/PXD3/PWM9/TS9	I/O	Digital/Analog	• GPIO35 • CIS: PXD3 • PWM9 (differential with PWM8) • Touch sensor 9
24	P36/PXD4/PWM10/TS10	I/O	Digital/Analog	• GPIO36 • CIS: PXD4 • PWM10 (differential with PWM11) • Touch sensor 10

Pin #	Name	I/O	Type	Description
25	P37/PXD5/PWM11/TS11	I/O	Digital/Analog	• GPIO37 • CIS: PXD5 • PWM11 (differential with PWM10) • Touch sensor 11
26	P47/1MISO/TS15/RGB0	I/O	Digital/Analog	• GPIO47 • SPI1: MISO • Touch sensor 15 • LCD: RGB0
27	P46/CAN_STB/1MOSI/TS14/RGB1	I/O	Digital/Analog	• GPIO46 • CAN STB: Transceiver standby mode (active high) • SPI1: MOSI • Touch sensor 14 • LCD: RGB1
28	P7/WIFI_ACT/PWM1/SYNC	I/O	Digital	• GPIO7 • Co-existence: WIFI ACTIVE • PWM1 (differential with PWM0) • I2S: SYNC
29	P6/CLK13M/PWM0/CLK	I/O	Digital	• GPIO6 • CLK13M: 26 MHz clock output (divide by 1/2/4/8) • PWM0 (differential with PWM1) • I2S: CLK
30	P5/2MISO/SD_D1	I/O	Digital	• GPIO5 • SPI2: MISO • SD: D1
31	P4/2MOSI/SD_D0	I/O	Digital	• GPIO4 • SPI2: MOSI • SD: D0
32	P3/2CSN/SD_CMD	I/O	Digital	• GPIO3 • SPI2: CSN • SD: CMD
33	P2/2SCK/SD_CLK	I/O	Digital	• GPIO2 • SPI2: SCK

Pin #	Name	I/O	Type	Description
				• SD: CLK
34	MICBIAS	-	Analog output	Microphone bias output
35	VCM	-	Analog output	Common mode voltage for audio
36	AUDRP	-	Analog output	Audio right channel positive output
37	AUDRN	-	Analog output	Audio right channel negative output
38	AUDLN	-	Analog output	Audio left channel negative output
39	AUDLP	-	Analog output	Audio left channel positive output
40	MICP2	-	Analog input	Microphone 2 positive input
41	MICN2	-	Analog input	Microphone 2 negative input
42	MICN1	-	Analog input	Microphone 1 negative input
43	MICP1	-	Analog input	Microphone 1 positive input
44	VDDRAM	-	Analog output	PSRAM LDO output
45	P38/PXD6/TS12	I/O	Digital/Analog	• GPIO38 • CIS: PXD6 • Touch sensor 12
46	P39/PXD7/TS13	I/O	Digital/Analog	• GPIO39 • CIS: PXD7 • Touch sensor 13
47	P19/SD_D3/RGB15	I/O	Digital	• GPIO19 • SD: D3 • LCD: RGB15
48	P14/SD_CLK/SCK/ANT0/RGB20	I/O	Digital	• GPIO14 • SD: CLK • SPI1: SCK • Bluetooth Antenna Selection 0 • LCD: RGB20
49	P16/SD_D0/MOSI/ANT2/RGB18	I/O	Digital	• GPIO16 • SD: D0 • SPI1: MOSI • Bluetooth Antenna Selection 2 • LCD: RGB18

Pin #	Name	I/O	Type	Description
50	P15/SD_CMD/CSN/ANT1/RGB19	I/O	Digital	• GPIO15 • SD: CMD • SPI1: CSN • Bluetooth Antenna Selection 1 • LCD: RGB19
51	P17/SD_D1/MISO/ANT3/RGB17	I/O	Digital	• GPIO17 • SD: D1 • SPI1: MISO • Bluetooth Antenna Selection 3 • LCD: RGB17
52	P18/SD_D2/RGB16	I/O	Digital	• GPIO18 • SD: D2 • LCD: RGB16
53	P24/CLK32K/PWM4/ADC2/IO0/RGB10	I/O	Digital/Analog	• GPIO24 • CLK32K: 32 kHz clock output • PWM4 (differential with PWM5) • ADC2 • QSPI: IO0 • LCD: RGB10
54	P26/TXEN/IO2/RGB8	I/O	Digital	• GPIO26 • TXEN is high when Wi-Fi RF is transmitting • QSPI: IO2 • LCD: RGB8
55	P23/DL_SO/ADC3/QCSN/RGB11	I/O	Digital/Analog	• GPIO23 • DL_SO: SO (SPI flash download) • ADC3 • QSPI: CSN • LCD: RGB11
56	P22/DL_SI/CLK26M/ADC5/QCLK/RGB12	I/O	Digital/Analog	• GPIO22 • DL_SI: SI (SPI flash download) • CLK26M: 26 MHz clock output • ADC5 • QSPI: CLK

Pin #	Name	I/O	Type	Description
				• LCD: RGB12
57	P21/DL_SCK/1SDA/SWDIO/ADC6/RGB13	I/O	Digital/Analog	• GPIO21 • DL_SCK: SCK (SPI flash download) • I2C1: SDA • SWDIO: SWD data • ADC6 • LCD: RGB13
58	P20/DL_CSN/1SCL/SWCLK/RGB14	I/O	Digital/Analog	• GPIO20 • DL_CSN: CSN (SPI flash download) • I2C1: SCL • SWCLK: SWD clock • LCD: RGB14
59	P45/CAN_RX/1CSN/ADC11/RGB2	I/O	Digital/Analog	• GPIO45 • CAN: RX • SPI1: CSN • ADC11 • LCD: RGB2
60	P44/CAN_TX/1SCK/ADC10/RGB3	I/O	Digital/Analog	• GPIO44 • CAN: TX • SPI1: SCK • ADC10 • LCD: RGB3
61	P43/2SDA/DOUT/RGB4	I/O	Digital	• GPIO43 • I2C2: SDA • I2S: DOUT • LCD: RGB4
62	P42/2SCL/DIN/RGB5	I/O	Digital	• GPIO42 • I2C2: SCL • I2S: DIN • LCD: RGB5
63	P8/BT_ACT/PWM2/DIN	I/O	Digital	• GPIO8 • Co-existence: Bluetooth ACTIVE • PWM2 (differential with PWM3) • I2S: DIN

Pin #	Name	I/O	Type	Description
64	P9/BT_PRIO/PWM3/DOUT	I/O	Digital	• GPIO9 • Co-existence: Bluetooth PRIOPRITY • PWM3 (differential with PWM2) • I2S: DOUT
65	P41/3TX/SYNC/RGB6	I/O	Digital	• GPIO41 • UART3: TX • I2S: SYNC • LCD: RGB6
66	P40/3RX/CLK/RGB7	I/O	Digital	• GPIO40 • UART3: RX • I2S: CLK • LCD: RGB7
67	WP_FLASH	-	Digital output	External flash write protect input
68	SO_FLASH	-	Digital input	External flash data output
69	CSN_FLASH	-	Digital output	External flash chip select
70	VDD_FLASH	-	Analog output	External flash power supply
71	HOLD_FLASH	-	Digital output	External flash hold input
72	SCK_FLASH	-	Digital output	External flash clock input
73	SI_FLASH	-	Digital output	External flash data input
74	P10/DL_1RX/SD_D2	I/O	Digital	• GPIO10 • UART1: RX (Flash download support) • SD: D2
75	P11/DL_1TX/SD_D3	I/O	Digital	• GPIO11 • UART1: TX (Flash download support) • SD: D3
76	P1/2RX/2SDA	I/O	Digital	• GPIO1 • UART2: RX • I2C2: SDA
77	P0/2TX/2SCL	I/O	Digital	• GPIO0 • UART2: TX • I2C2: SCL

Pin #	Name	I/O	Type	Description
78	XI	-	Analog input	26 MHz crystal input
79	XO	-	Analog output	26 MHz crystal output
80	VCCPLL	-	Analog input	RF PLL power supply
Die pad	GND_SLUG	-	GND	Ground

3.2 QFN68 Pin Description

Figure 3-2 shows the pin assignments of the 8 x 8 mm, 68-pin QFN package.

Figure 3-2 QFN68 Pin Assignments

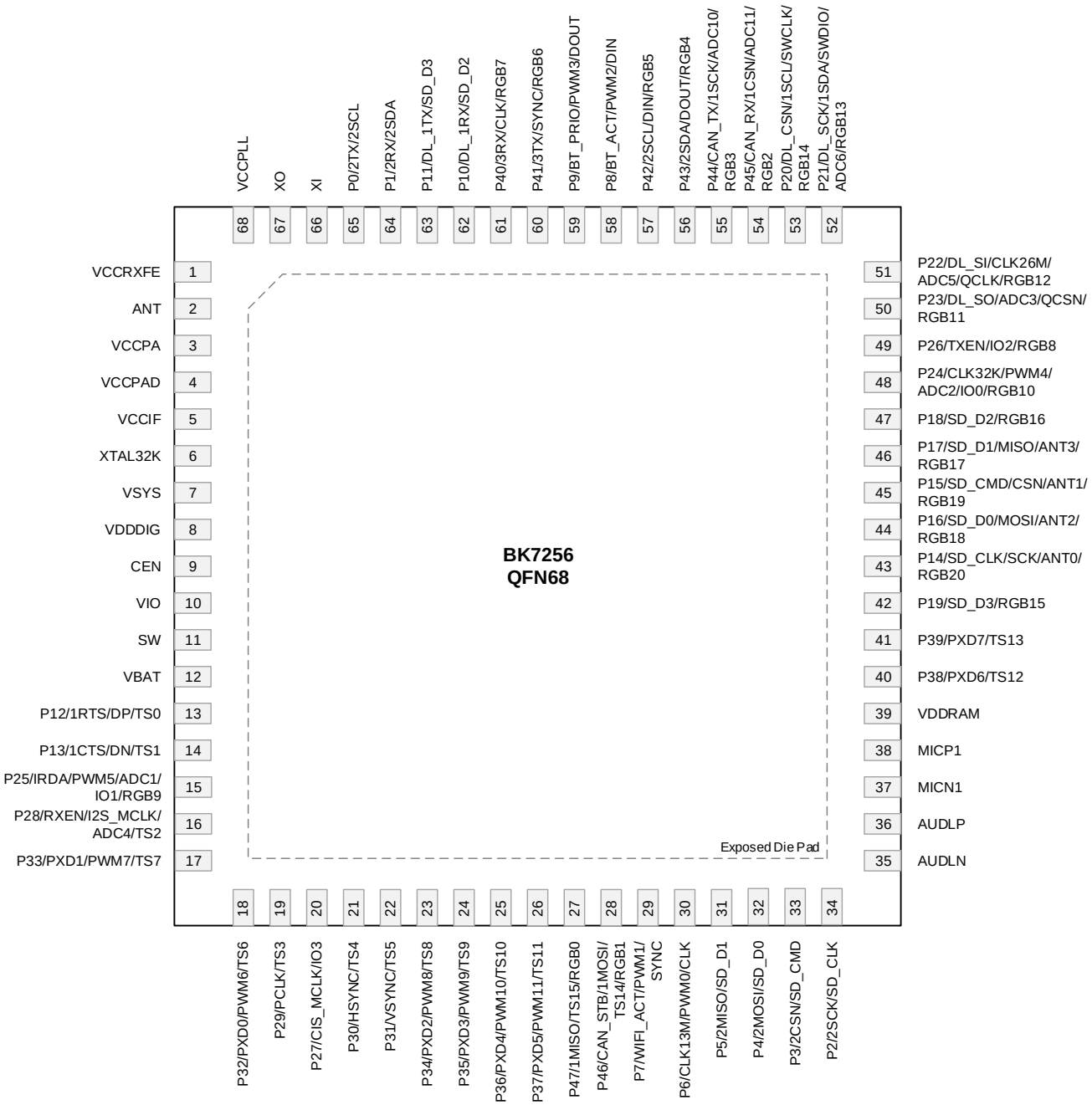


Table 3-2 shows the pin descriptions of the QFN68 package.

Table 3-2 QFN68 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port
3	VCCPA	-	Analog input	RF PA power supply
4	VCCPAD	-	Analog input	RF PA driver power supply
5	VCCIF	-	Analog input	IF power supply
6	XTAL32K	-	Analog input	32.768 kHz crystal input
7	VSYS	-	Analog output	System LDO output
8	VDDDIG	-	Analog output	Digital LDO output
9	CEN	-	Analog input	Chip enable, active high
10	VIO	-	Analog output	IO LDO/BUCK output
11	SW	-	BUCK output	BUCK switch output
12	VBAT	-	Power	Chip power supply
13	P12/1RTS/DP/TS0	I/O	Digital/Analog	• GPIO12 • UART1: RTS • USB: DP • Touch sensor 0
14	P13/1CTS/DN/TS1	I/O	Digital/Analog	• GPIO13 • UART1: CTS • USB: DN • Touch sensor 1
15	P25/IRDA/PWM5/ADC1/IO1/RGB9	I/O	Digital/Analog	• GPIO25 • IrDA TX/RX • PWM5 (differential with PWM4) • ADC1 • QSPI: IO1 • LCD: RGB9
16	P28/RXEN/I2S_MCLK/ADC4/TS2	I/O	Digital/Analog	• GPIO28 • RXEN is high when Wi-Fi RF is receiving • I2S: MCLK

Pin #	Name	I/O	Type	Description
				• ADC4 • Touch sensor 2
17	P33/PXD1/PWM7/TS7	I/O	Digital/Analog	• GPIO33 • CIS: PXD1 • PWM7 (differential with PWM6) • Touch sensor 7
18	P32/PXD0/PWM6/TS6	I/O	Digital/Analog	• GPIO32 • CIS: PXD0 • PWM6 (differential with PWM7) • Touch sensor 6
19	P29/PCLK/TS3	I/O	Digital/Analog	• GPIO29 • CIS: PCLK • Touch sensor 3
20	P27/CIS_MCLK/IO3	I/O	Digital/Analog	• GPIO27 • CIS: MCLK • QSPI: IO3
21	P30/HSYNC/TS4	I/O	Digital/Analog	• GPIO30 • CIS: HSYNC • Touch sensor 4
22	P31/VSYNC/TS5	I/O	Digital/Analog	• GPIO31 • CIS: VSYNC • Touch sensor 5
23	P34/PXD2/PWM8/TS8	I/O	Digital/Analog	• GPIO34 • CIS: PXD2 • PWM8 (differential with PWM9) • Touch sensor 8
24	P35/PXD3/PWM9/TS9	I/O	Digital/Analog	• GPIO35 • CIS: PXD3 • PWM9 (differential with PWM8) • Touch sensor 9
25	P36/PXD4/PWM10/TS10	I/O	Digital/Analog	• GPIO36 • CIS: PXD4 • PWM10 (differential with PWM11) • Touch sensor 10

Pin #	Name	I/O	Type	Description
26	P37/PXD5/PWM11/TS11	I/O	Digital/Analog	• GPIO37 • CIS: PXD5 • PWM11 (differential with PWM10) • Touch sensor 11
27	P47/1MISO/TS15/RGB0	I/O	Digital/Analog	• GPIO47 • SPI1: MISO • Touch sensor 15 • LCD: RGB0
28	P46/CAN_STB/1MOSI/TS14/ RGB1	I/O	Digital/Analog	• GPIO46 • CAN STB: Transceiver standby mode (active high) • SPI1: MOSI • Touch sensor 14 • LCD: RGB1
29	P7/WIFI_ACT/PWM1/SYNC	I/O	Digital	• GPIO7 • Co-existence: WIFI ACTIVE • PWM1 (differential with PWM0) • I2S: SYNC
30	P6/CLK13M/PWM0/CLK	I/O	Digital	• GPIO6 • CLK13M: 26 MHz clock output (divide by 1/2/4/8) • PWM0 (differential with PWM1) • I2S: CLK
31	P5/2MISO/SD_D1	I/O	Digital	• GPIO5 • SPI2: MISO • SD: D1
32	P4/2MOSI/SD_D0	I/O	Digital	• GPIO4 • SPI2: MOSI • SD: D0
33	P3/2CSN/SD_CMD	I/O	Digital	• GPIO3 • SPI2: CSN • SD: CMD
34	P2/2SCK/SD_CLK	I/O	Digital	• GPIO2 • SPI2: SCK

Pin #	Name	I/O	Type	Description
				• SD: CLK
35	AUDLN	-	Analog output	Audio left channel negative output
36	AUDLP	-	Analog output	Audio left channel positive output
37	MICN1	-	Analog input	Microphone 1 negative input
38	MICP1	-	Analog input	Microphone 1 positive input
39	VDDRAM	-	Analog output	PSRAM LDO output
40	P38/PXD6/TS12	I/O	Digital/Analog	• GPIO38 • CIS: PXD6 • Touch sensor 12
41	P39/PXD7/TS13	I/O	Digital/Analog	• GPIO39 • CIS: PXD7 • Touch sensor 13
42	P19/SD_D3/RGB15	I/O	Digital	• GPIO19 • SD: D3 • LCD: RGB15
43	P14/SD_CLK/SCK/ANT0/ RGB20	I/O	Digital	• GPIO14 • SD: CLK • SPI1: SCK • Bluetooth Antenna Selection 0 • LCD: RGB20
44	P16/SD_D0/MOSI/ANT2/RGB18	I/O	Digital	• GPIO16 • SD: D0 • SPI1: MOSI • Bluetooth Antenna Selection 2 • LCD: RGB18
45	P15/SD_CMD/CSN/ANT1/ RGB19	I/O	Digital	• GPIO15 • SD: CMD • SPI1: CSN • Bluetooth Antenna Selection 1 • LCD: RGB19
46	P17/SD_D1/MISO/ANT3/RGB17	I/O	Digital	• GPIO17 • SD: D1 • SPI1: MISO

Pin #	Name	I/O	Type	Description
				• Bluetooth Antenna Selection 3 • LCD: RGB17
47	P18/SD_D2/RGB16	I/O	Digital	• GPIO18 • SD: D2 • LCD: RGB16
48	P24/CLK32K/PWM4/ADC2/IO0/ RGB10	I/O	Digital/Analog	• GPIO24 • CLK32K: 32 kHz clock output • PWM4 (differential with PWM5) • ADC2 • QSPI: IO0 • LCD: RGB10
49	P26/TXEN/IO2/RGB8	I/O	Digital	• GPIO26 • TXEN is high when Wi-Fi RF is transmitting • QSPI: IO2 • LCD: RGB8
50	P23/DL_SO/ADC3/QCSN/ RGB11	I/O	Digital/Analog	• GPIO23 • DL_SO: SO (SPI flash download) • ADC3 • QSPI: CSN • LCD: RGB11
51	P22/DL_SI/CLK26M/ADC5/ QCLK/RGB12	I/O	Digital/Analog	• GPIO22 • DL_SI: SI (SPI flash download) • CLK26M: 26 MHz clock output • ADC5 • QSPI: CLK • LCD: RGB12
52	P21/DL_SCK/1SDA/SWDIO/ ADC6/RGB13	I/O	Digital/Analog	• GPIO21 • DL_SCK: SCK (SPI flash download) • I2C1: SDA • SWDIO: SWD data • ADC6 • LCD: RGB13
53	P20/DL_CSN/1SCL/SWCLK/ RGB14	I/O	Digital/Analog	• GPIO20

Pin #	Name	I/O	Type	Description
				• DL_CSN: CSN (SPI flash download) • I2C1: SCL • SWCLK: SWD clock • LCD: RGB14
54	P45/CAN_RX/1CSN/ADC11/ RGB2	I/O	Digital/Analog	• GPIO45 • CAN: RX • SPI1: CSN • ADC11 • LCD: RGB2
55	P44/CAN_TX/1SCK/ADC10/ RGB3	I/O	Digital/Analog	• GPIO44 • CAN: TX • SPI1: SCK • ADC10 • LCD: RGB3
56	P43/2SDA/DOUT/RGB4	I/O	Digital	• GPIO43 • I2C2: SDA • I2S: DOUT • LCD: RGB4
57	P42/2SCL/DIN/RGB5	I/O	Digital	• GPIO42 • I2C2: SCL • I2S: DIN • LCD: RGB5
58	P8/BT_ACT/PWM2/DIN	I/O	Digital	• GPIO8 • Co-existence: Bluetooth ACTIVE • PWM2 (differential with PWM3) • I2S: DIN
59	P9/BT_PRIO/PWM3/DOUT	I/O	Digital	• GPIO9 • Co-existence: Bluetooth PRIOPRITY • PWM3 (differential with PWM2) • I2S: DOUT
60	P41/3TX/SYNC/RGB6	I/O	Digital	• GPIO41 • UART3: TX • I2S: SYNC • LCD: RGB6

Pin #	Name	I/O	Type	Description
61	P40/3RX/CLK/RGB7	I/O	Digital	• GPIO40 • UART3: RX • I2S: CLK • LCD: RGB7
62	P10/DL_1RX/SD_D2	I/O	Digital	• GPIO10 • UART1: RX (Flash download support) • SD: D2
63	P11/DL_1TX/SD_D3	I/O	Digital	• GPIO11 • UART1: TX (Flash download support) • SD: D3
64	P1/2RX/2SDA	I/O	Digital	• GPIO1 • UART2: RX • I2C2: SDA
65	P0/2TX/2SCL	I/O	Digital	• GPIO0 • UART2: TX • I2C2: SCL
66	XI	-	Analog input	26 MHz crystal input
67	XO	-	Analog output	26 MHz crystal output
68	VCCPLL	-	Analog input	RF PLL power supply
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 Modes of Operation

The BK7256 supports four low-power modes except active mode, namely shutdown mode, deep sleep mode, low voltage standby mode and normal standby mode, where shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the always-on (AON) logic and GPIO. Any GPIO edge transition or RTC event can power up the system again. Retention registers can keep their contents.

Low Voltage Standby Mode: The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, thus the current is much lower. Only the RTC and GPIOs can bring the system back to active mode with normal voltage.

Normal Standby Mode: The MCU stops running and all peripheral interrupts can resume the MCU.

Active Mode: The MCU is active and all peripherals are available.

4.2 Wi-Fi/Bluetooth Transceiver

The BK7256 integrates a high-performance Wi-Fi/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended input and transforms the amplified signal into a differential output to achieve better noise and linearity trade-off. On the transmit side, the differential output of the power amplifier (PA) is combined and transformed to a single-ended output using the on-chip balun. This enables only one ANT pin connection to the antenna for both transmit and receive operations. The communication range can be extended by configuring GPIO26 and GPIO28 as TXEN and RXEN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.3 Bluetooth and WLAN Coexistence

The built-in packet traffic arbitration (PTA) ensures stable Bluetooth and Wi-Fi dual connectivity and enables efficient sharing of over-the-air resources.

4.4 Clock Management

The clock sources available in the BK7256 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator (X26M), using external 26 MHz crystal
  - 26 ~ 240 MHz digitally controlled oscillator (DCO) with 1% variation after calibration
  - 320/480 MHz PLL (DPLL)
- Low-frequency clocks
  - 32.768 kHz crystal oscillator (X32K), using external 32.768 kHz crystal
  - 32 kHz ring oscillator (ROSC)
  - 32 kHz (32.768 kHz) derived from X26M (D32K)
- Audio clock
  - Audio PLL with a default frequency of 98.304 MHz (APLL)

The clock selection options for MCU and peripherals are listed as follows.

Table 4-1 Clock Selection

MCU and Peripherals	X26M	DCO	DPLL	LPO_CLK[a]	APLL
MCU	√	√	√		
FLASH Controller	√		√		√
SPI1	√				√
SPI2	√				√
QSPI			√		
UART1	√				√
UART2	√				√
UART3	√				√
SD/SDIO	√		√		
I2C1	√				
I2C2	√				
USB			√		
CAN	√				
GDMA	√	√	√		
DMA2D	√	√	√		
LCD			√		

MCU and Peripherals	X26M	DCO	DPLL	LPO_CLK[a]	APLL
JPEG			√		
CIS DVP Camera			√		
PWM	√			√	
I2S	√				√
Audio ADC	√				√
Audio DAC	√				√
SAR ADC	√				√
TIMER0	√			√	
TIMER1	√			√	
Main watchdog				√	
AON watchdog				√	
RTC				√	
IrDA	√				

a. The low-power clock (LPO_CLK) can be derived from X32K, D32K or ROSC.

The system also has clock output capability to output clock signals to external components.

- The LPO_CLK and X26M clock can be output to GPIOs for general purpose.
- The clock derived from X26M (divide by 1/2/4/8) can be output to GPIOs for general purpose.

4.5 Reset

A reset can be triggered by the following sources: Power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

System power on, digital power on and watchdog reset have the same reset effect on major blocks except the always-on logic, that any reset will reset the whole chip to its initial status. The always on logic has one 32-bit timer and 16-bit retention registers, which can only be reset to initial values by system power on reset.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power down mode, which triggers the whole system reset procedure.

4.6 Power Management

The power management system on the BK7256 includes a buck converter and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The BK7256 can be powered from an external power supply ranging from 2.7 V to 5.0 V via the VBAT pin. The BK7256 can operate in buck or LDO mode. When operating in buck mode, all modules are supplied from the buck converter. When operating in LDO mode, all modules are supplied from the IO LDO regulator.

Note: Outputs from the buck converter and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the BK7256 EVB User Guide and application note for more details about choosing the proper bypass capacitors.

4.7 GPIO

The BK7256 has up to 48 GPIOs which can be configured as either input or output. All GPIOs have alternate functions.

All GPIO pins can wake up the internal MCU from deep sleep mode. In deep sleep mode, any level change on the set GPIO will trigger the wake-up procedure.

4.8 SPI

The BK7256 integrates two SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 30 MHz in master mode and 30 MHz in slave mode. The SPI interfaces support a configurable 8-bit or 16-bit data width, 4-wire and 3-wire mode (without CSN pin), as well as a 64-depth RX FIFO and a 64-depth TX FIFO with DMA capability.

The reception data can be latched on either the rising or falling edge of the clock signal. The SPI interfaces can send data with MSB first or LSB first.

4.9 QSPI

The BK7256 embeds a Quad SPI interface that provides support for communicating with external flash, PSRAM or AMOLED display. The QSPI allows communicating up to 80 MHz.

4.10 UART

The BK7256 includes three Universal Asynchronous Receiver/Transmitter (UART) interfaces, UART1, UART2 and UART3, which support full-duplex, asynchronous serial communication at a baud rate up to 2 Mbps. They support 5/6/7/8-bit data, and even, odd or none parity check. The stop bit can be either 1 bit or 2 bits.

UART1 supports hardware flow control with RTS and CTS signal. UART1 also supports Flash download.

Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.

4.11 SD/SDIO

A SD/SDIO host/slave interface is available on the BK7256. The SD/SDIO interface is SD memory version 2.0 and SDIO version 2.0 compliant. The SD/SDIO interface allows a maximum 40 MHz clock speed and supports two different data bus modes, 1 bit (default) and 4 bits. It can be used as a host to read external SD cards or used by external host as a slave to communicate with chips.

The SD/SDIO interface supports DMA capabilities, allowing high-speed transfer without MCU load.

4.12 I2C

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7256 embeds two I2C interfaces, which can operate in Master or Slave mode. They support standard (up to 100 kbps) and fast (up to 400 kbps) modes with 7-bit addressing. If a low level applied on SCL or the duration the bus is idle is greater than a programmable threshold, it will generate interrupt to MCU.

4.13 USB

The BK7256 embeds an USB On-The-Go (OTG) full-speed controller with an integrated transceiver. The USB controller is compliant with the USB 1.1 and 2.0 specification. It can operate as a host or a device and supports full-speed (FS) operation (up to 12 Mbps).

The device supports 7 endpoints in addition to control endpoint 0. Endpoints 1-7 can be configured as IN or OUT and support bulk, interrupt, and isochronous data transfer. The controller has a FIFO of 2K bytes, which can be allocated to the 8 endpoints as configured.

4.14 CAN

The BK7256 embeds a Controller Area Network (CAN) controller that uses the basic CAN principle and meets all constraints of the CAN-specification 2.0B active. Furthermore, the CAN controller can be configured to meet the specification of CAN with flexible data rate CAN FD. CAN 2.0 carries a data payload up to 8 bytes and CAN FD up to 64 bytes.

4.15 GDMA

The BK7256 has a general-purpose DMA controller (GDMA) with 12 DMA channels to unload CPU activity. The six channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word) or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

A selection of peripherals on the BK7256 have DMA capabilities, including UART1, SPI1, SDIO, UART2, UART3, SPI2, USB, audio, I2S, LCD, and JPEG.

4.16 DMA2D

The BK7256 has a specialized DMA controller (DMA2D) dedicated to image processing, offering direct memory transfer and 2D graphical acceleration without CPU intervention. It can perform the following operations:

- Filling a part or the whole of a destination image with a fixed color
- Copying a part or the whole of a source image into a part or the whole of a destination image
- Copying a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blending a part or two complete source images with a different pixel format and copying the result into a part or the whole of a destination image with a different color format

The DMA2D controller supports six operating modes:

- Register to memory
- Memory to memory
- Memory to memory with pixel format conversion
- Memory to memory with pixel format conversion and blending
- Memory to memory with pixel format conversion, blending and fixed color foreground layer

- Memory to memory with pixel format conversion, blending and fixed color background layer

Up to 11 color modes are supported from 4-bit up to 32-bit per pixel with indexed or direct color coding. The DMA2D features dedicated memories for color lookup table (CLUT) storage.

An interrupt can be generated on the following events:

- Configuration error
- CLUT transfer completion
- CLUT access error
- Watermark on a user programmable destination line
- Transfer completion
- Transfer error

4.17 LCD

The BK7256 supports a LCD-TFT display controller capable of providing a 16-bit parallel digital RGB (Red, Green, Blue) or a I8080 interface. The controller supports conversion from YUV420 to RGB565 in RGB display.

Table 4-2 Display Pins and External Signal Interface

GPIO	LCD Signals (I/O)	RGB565 Interface	RGB888 Interface	I8080 Interface
GPIO14	LCD_RGB[20] (O)	DCLK	DCLK	NC
GPIO15	LCD_RGB[19] (O)	DISP	DISP	NC
GPIO16	LCD_RGB[18] (O)	DE	DE	NC
GPIO17	LCD_RGB[17] (O)	HSYNC	HSYNC	NC
GPIO18	LCD_RGB[16] (O)	VSYNC	VSYNC	NC
GPIO19	LCD_RGB[15] (O)	R4	R7	CSX
GPIO20	LCD_RGB[14] (O)	R3	R6	RESET
GPIO21	LCD_RGB[13] (O)	R2	R5	RSX
GPIO22	LCD_RGB[12] (O)	R1	R4	WRX
GPIO23	LCD_RGB[11] (O)	R0	R3	RDX
GPIO24	LCD_RGB[10] (O)	G5	G7	NC
GPIO25	LCD_RGB[9] (O)	G4	G6	NC
GPIO26	LCD_RGB[8] (O)	G3	G5	NC

GPIO	LCD Signals (I/O)	RGB565 Interface	RGB888 Interface	I8080 Interface
GPIO40	LCD_RGB[7] (O)	G2	G4	D7
GPIO41	LCD_RGB[6] (O)	G1	G3	D6
GPIO42	LCD_RGB[5] (O)	G0	G2	D5
GPIO43	LCD_RGB[4] (O)	B4	B7	D4
GPIO44	LCD_RGB[3] (O)	B3	B6	D3
GPIO45	LCD_RGB[2] (O)	B2	B5	D2
GPIO46	LCD_RGB[1] (O)	B1	B4	D1
GPIO47	LCD_RGB[0] (O)	B0	B3	D0

4.18 JPEG

The BK7256 embeds a JPEG encoder/decoder that can encode and decode a JPEG stream. It provides a small hardware compressor and a decompression accelerator of JPEG images. The JPEG encoder supports up to 32 programmable quantization tables.

4.19 Camera Interface

The 8-bit CMOS Image Sensor (CIS) Digital Video Port (DVP) camera interface provides 8-bit parallel port interface to a sensor, together with main clock (MCLK), pixel clock (PCLK), Horizontal SYNC (HSYNC) and Vertical SYNC (VSYNC) signals. Supported sensors could be but not limited to OV7676, OV7670, GC0308, GC0309, GC0329 and PAS6329.

The YUV sensor’s input will be directly fed to the hardware JPEG encoder, and the JPEG encoder output will be write to data memory directly by a dedicated DMA channel.

The YUV signal format can be YUYV, UYVY, YYUV and UVYY. HSYNC and VSYNC level can be set independently.

4.20 PWM

The BK7256 has up to 12 32-bit PWM channels, labeled PWM0 ~ 11 (Timer mode supported). Each PWM channel has three modes: Timer mode, PWM mode, and Capture mode. Each mode of each channel is multiplexed with a 32-bit counter. The PWM running clock can be either high-speed clock or low-power clock. Each PWM runs independently with its own duty cycle.

The main features of the PWM module are listed here:

- Fixed PWM base frequency with programmable prescaler (1 ~ 256)
- The counter increases in one direction, and it automatically continues counting from 0 when it overflows to the maximum value.
- Each channel can be individually enabled, and the mode of each channel can be individually configured.
- Capable of continuous counting between two rising edges, two falling edges or dual edges in Capture mode
- Configurable PWM period and duty-cycle for each PWM channel
- Real-time count value can be read in Timer mode.

4.20.1 Timer Mode

In Timer mode, the counter is enabled and incrementally counted, and an interrupt is generated when the specified cycle value is reached. Counting restarts from 0.

If the software refreshes the count cycle value during the counting process, the new count cycle value is used as the count cycle. If the current count value is greater than the new count cycle value, it resets to 0 and starts over.

The counter resets to 0 immediately if Enable = 0. If Stop = 1, the counter stops incrementing and remains its current state, and continues counting after Stop = 0.

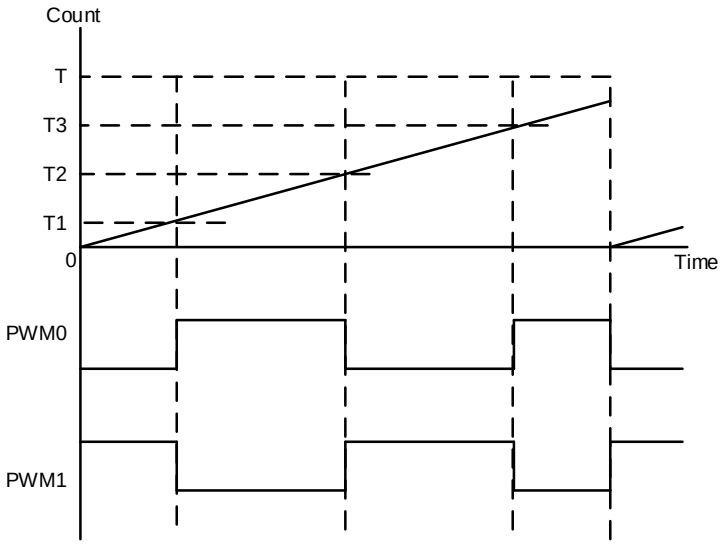
The current count value of the counter can be read in real time.

4.20.2 PWM Mode

In PWM mode, the PWM waveform start level can be configured as 0 or 1. The waveform timing is configured with four parameters.

- Waveform period T (1~2^32)
- The first level inversion time T1 (0~2^32-1, 0 - no inversion)
- The second level inversion time T2 (0~2^32-1, 0 - no inversion)
- The third level inversion time T3 (0~2^32-1, 0 - no inversion)

The PWM channels can be configured in six pairs. When two adjacent channels are configured in paired mode, their start-up time is aligned, and, at that point, the waveform period must be configured to the same value.



As shown in the above figure, PWM0 and PWM1 have opposite start levels, share same waveform parameters, and are in paired mode.

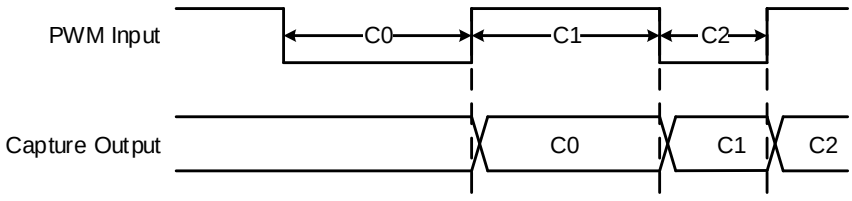
In PWM mode, no interrupts are generated.

During operation, any updates to the configuration parameters will take no effect until the next time the counter starts from 0 again.

4.20.3 Capture Mode

Capture mode, which uses the operating clock to count the time between input signal edges, has the following three modes of edges:

- Rising edge: between two rising edges
- Falling edge: between two falling edges
- Dual edge: between any two edges



The figure above shows the Capture result between dual edges.

Each time there is an update to the Capture output, an interrupt is generated. The software must read out the Capture result before the next update, otherwise the Capture result will be overwritten by the new result.

4.21 I2S

The BK7256 integrates a I2S interface. The I2S interface supports master and slave mode with sample rates from 8 kHz to 384 kHz.

The I2S interface supports both PCM mono channel mode and I2S stereo channel mode. The data width can be 1 to 32 bits.

4.22 Audio Peripherals

The BK7256 comes with a rich set of audio peripherals to enhance the listening experience. The chip includes a four-band digital equalizer, two analog-to-digital converters (ADC), two digital-to-analog converters (DAC), two microphone input amplifiers, and two audio amplifiers, as well as a SBC decoder accelerator.

4.22.1 Four-Band Digital Equalizer

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption. The four-band equalizer can be easily configured by using the BK7256 software configuration tool kit. For more information, refer to the BK7256 Software Configuration Tool User Guide.

4.22.2 Audio ADC and DAC

The BK7256 contains two high fidelity ADCs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates two high fidelity DACs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz.

4.22.3 Microphone Input Amplifier

The BK7256 contains two fully differential analog microphone input amplifiers, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with gain from 0 to 32 dB with 2 dB step.

4.22.4 Audio Amplifier

The BK7256 provides two high quality audio amplifiers capable of driving 16 Ω speakers with load capacitance up to 30 pF.

4.23 General Purpose SAR ADC

The BK7256 embeds a 13-bit general-purpose SAR ADC with programmable sampling rates from 12.5 kHz up to 1.625 MHz. The 13-bit resolution ADC can be configured to 15 ~ 17 bits.

The ADC supports up to eight external input channels. It can operate in one-shot mode, software control mode or continuous mode. The ADC supports full scale input range (0 V to 2*VREF).

Table 4-3 SAR ADC Input Channel

Channel Number	Detected Voltage	Description
0	VBAT	Monitor battery voltage (0.4*VBAT)
1	ADC1	GPIO25 voltage
2	ADC2	GPIO24 voltage
3	ADC3	GPIO23 voltage
4	ADC4	GPIO28 voltage
5	ADC5	GPIO22 voltage
6	ADC6	GPIO21 voltage
7	Temperature sensor	Temperature sensor output voltage
10	ADC10	GPIO44 voltage
11	ADC11	GPIO45 voltage

4.24 General-Purpose Timers

The BK7256 includes two general-purpose timers, TIMER0 and TIMER1, and each timer has three 32-bit timer channels. Each timer can choose a 26 MHz clock or a 32 kHz clock as the main clock. Each timer has three 32-bit counters and a 4-bit pre-divider.

4.25 Watchdogs

The BK7256 has two watchdogs. The main watchdog runs on a slow clock divided by a 32 kHz clock (factor 1/2/4/8/16) and has a maximum programmable period of up to 32.768 (2^16/2 kHz) seconds. The watchdog in the always-on domain runs on ROSC an d has a maximum programmable period of up to 2.048 (2^16/32 kHz) seconds.

4.26 Real-Time Counter (RTC)

The real-time counter (RTC) module features a 32-bit counter and a tick event generator. The RTC runs on a 32 kHz clock derived from X32K, D32K or ROSC. It is used for low-power timing, and it can keep running even when the system is in low-voltage standby.

4.27 IrDA

The BK7256 embeds a hardware IrDA interface to encode and decode the signal. In addition, the interface has the capture timer capability to allow software decoding of input signals.

4.28 Temperature Sensor

The BK7256 integrates an on-chip temperature sensor. The temperature sensor can measure on-chip temperature over -40 to +125 ℃ with an accuracy of ±5 ℃. The digital results can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce the transmit power or suspend operation at high temperatures.

4.29 Touch Sensor

The BK7256 has up to 16 capacitive-sensing GPIOs, labeled TS0 ~ 15, which detect capacitance changes induced by touch or proximity of objects immediately.

4.30 Secure Element

The BK7256 provides state-of-the-art security based on a powerful security architecture. It offers platform Root of Trust (RoT) based on an isolated Secure Element (SE). SE is a module that protects valuable assets, such as secret keys for embedded security sensitive applications in a Trusted Execution Environment (TEE). Using a dedicated hardware module increases security level and performance compared to a cryptographic software library.

The OTP, ROM and other memories inside SE allow for the secure storage of key material and other security sensitive data (assets). With functions including key derivation, non-volatile countermanagement, secure storage, asset management and a variety of cipher and hash operations, SE acts as a vault within the embedded system. The assets are referenced by authorized users, which increases security and prevents unauthorized use and abuse.

SE embeds hardware implementations of cryptographic algorithms that support various operations and modes required by applications in a TEE.

The SE inside BK7256 is FIPS 140-2 Level 2 certified and supports all security features required for FIPS 140-2 Level 2 certification. It embeds the following algorithms:

- RSA, ECDSA
- DRBG
- Triple-DES (ECB, CBC)
- AES (ECB, CBC, CTR, XTS)
- AES-CCM, AES-CMAC
- HMAC, SHS for SHA-1, SHA-224/256 and SHA-384/512
- SM2, SM3, SM4
- Poly1305, Chacha20
- KDF

Asset Store

The Asset Store is a securely managed memory that can store sensitive security parameters. The memory is on-chip SRAM embedded in the SE.

- Employs a safe-deposit box system that only allows asset use according to the associated ownership and policy of the asset
- Ownership keeps assets from different applications and different Hosts separated:
  - CPU Identity: 2-bit and 1-bit Normal/Secure world
  - Application Identity: 32 bits
  - Application Long-term Identity: 33 up to 224 bytes
- Root Key based security via OTP interface
- Supports symmetric and asymmetric key storage and export using AES SIV key-blobs
- Symmetric key generation and derivation using NIST SP 800-108 algorithm:
  - Derive a KDK from a Root Key
  - Derive a KEK from a Root Key
  - Derive a Key Asset from a KDK
- Shared secret generation based on asymmetric key exchange
- KDF NIST SP 800-56A & B – HMAC and CMAC based
- Key derivation according to NIST SP 800-135. Authentication allows access control to assets.

- Authorization based on authentication state

Timers

- Time stamping of keys
- Key lifetime and access window management based on timestamp
- Functions are based on hardware timers in a dedicated clock domain.

True Random Number Generator (TRNG)

- FIPS 140-2&3/SP 800-90 compliant
- Hardware-based, non-deterministic RNG
- Used to internally generate session keys, IVs, nonces, cookies, public and private keys
- Random Number Generation using SP 800-90 NRBG, SHA-2 conditioning and AES-256 CTR_DRBG

Public Key Accelerator

- Hardware accelerated public key operations for secure boot using ECDSA-P256/P384
- Signing and verifying using RSA-PSS, RSA-PKCS#1.5 and ECDSA
- Basic operations for DH, DSA, ECDSA, RSA and SM2, including:
  - ECDH
  - ECDSA-P256 and ECDSA-P384
  - RSA-1024, RSA-2048, RSA-3072 and Curve25519 support
  - SM2

Crypto Algorithms

- DES, TDES
  - ECB, CBC
- AES
  - ECB, CBC, CTR, ICM, f8, XTS
  - CMAC, CCM, GCM
  - Wrap and unwrap (NIST SP800-38F)
  - Key lengths: 128, 192 and 256 bits
- ChaCha20
  - Key lengths: 128 and 256 bits
- SM4
  - Key length: 128 bits

Hash Algorithms

- Basic hash and HMAC modes
  - MD5
  - SHA-1
  - SHA-224 and SHA-256
  - SHA-384 and SHA-512
  - Poly1305
  - SM3-512

Management of Non-Volatile Assets

- Root of Trust
- Provisioning/personalization
- Monotonic counters:
  - Short monotonic counters can be stored internally in OTP (up to 127 states) and can be used for host firmware version numbering or other infrequently updated counters.
  - Long monotonic counters must be stored externally in non-volatile system memory.
- Private to the crypto module, read and write access
- One Time Programmable (OTP) memory management and access:
  - Up to 28 data objects:
    - Static Asset (private to Asset Store)
    - Authentication Key Asset (private to Asset Store)
    - Trusted firmware version and other short non-volatile counters
    - Public Data (can be requested via Token Interface)
  - Trusted firmware version management by (short) monotonic counters
  - OTP write protection by OTP status bits
  - Partially programmed in the factory during device production

Secure Debug

- Enables host system level secure debugging
- Bits can be enabled/disabled under the control of public key cryptography.

Secure Boot

- Image decryption:
  - AES-CBC or AES-CTR depending on the use case

- Image signature verification:
  - ECDSA NIST P-256/384
  - SHA-256
- Helper functions:
  - Symmetric key generation
  - Key derivation
  - AES wrap

Embedded Controller

- Flexibility through programmability
- ROM based firmware program memory ensures system security.

Host Command Interface

- Token based command interface
- Four separate mailboxes for commands
- The commands and results of Normal (Non-secure) and Secure world are separated and cannot be accessed by the other world.

5. Electrical Characteristics

Note: Values currently listed in this section are preliminary measurements and are subject to change.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Battery regulator supply voltage	-0.3	5.0	V
VCCIF	Supply voltage for IF	-0.3	3.6	V
VCCRXFE	Supply voltage for RX	-0.3	3.6	V
VCCPA	Supply voltage for PA	-0.3	3.6	V
VCCPAD	Supply voltage for PA driver	-0.3	3.6	V
VCCPLL	Supply voltage for RF PLL	-0.3	3.6	V
VDDDIG	Digital LDO output voltage	-0.3	1.3	V
VSYS	System LDO output voltage	-0.3	3.6	V
VIO	IO LDO/BUCK output voltage	-0.3	3.6	V
VDDRAM	PSRAM LDO output voltage	-0.3	3.6	V
VDD_FLASH	Supply voltage for external flash	-0.3	2.0	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-40	150	℃

5.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Battery regulator supply voltage	2.7	-	5.0	V
VCCIF	Supply voltage for IF	2.7	-	3.6	V
VCCRXFE	Supply voltage for RX	2.7	-	3.6	V
VCCPA	Supply voltage for PA	2.7	-	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VCCPAD	Supply voltage for PA driver	2.7	-	3.6	V
VCCPLL	Supply voltage for RF PLL	2.7	-	3.6	V
VDDDIG	Digital LDO output voltage	1.0	1.1	1.2	V
VSYS	System LDO output voltage	2.4	-	3.2	V
VIO	IO LDO/BUCK output voltage	2.7	-	3.6	V
VDDRAM	PSRAM LDO output voltage	2.7	-	3.6	V
VDD_FLASH	Supply voltage for external flash	-	1.8	-	V
T_{OPR}	Operating temperature range	-40	-	125	℃

5.3 Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO/BUCK output voltage	2.7	3.2	3.6	V
Load current	-	-	-	150	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz

5.4 System LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VSYS	System LDO output voltage	2.4	3.0	3.2	V
Load current	-	-	-	150	mA

5.5 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital LDO output voltage	1.0	1.1	1.2	V
Load current	-	-	-	100	mA

5.6 Crystal and Reference Clock

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	Crystal and reference frequency	-	26	-	MHz
Tolerance	Crystal and reference frequency tolerance	-10	-	+10	ppm

5.7 Current Consumption

Measured with T = 25 ℃, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11b: 11 Mbps DSSS	-	63	-	mA
	11g: 54 Mbps OFDM	-	69	-	mA
	11n: MCS7, HT20	-	69	-	mA
	11n: MCS7, HT40	-	TBD	-	mA
	11ax: MCS7, HE20	-	TBD	-	mA
TX current	11b: 11 Mbps DSSS @ 17 dBm	-	280	-	mA
	11g: 54 Mbps OFDM @ 15 dBm	-	250	-	mA
	11n: MCS7, HT20 @ 14 dBm	-	250	-	mA
	11n: MCS7, HT40 @ 14 dBm	-	TBD	-	mA
	11ax: MCS7, HE20 @ 14 dBm	-	TBD	-	mA
Standby Mode					
Normal standby	-	-	3.0	-	mA
Low voltage standby	-	-	150	-	µA
Deep Sleep Mode					
Deep sleep	-	-	15	-	µA
Shutdown Mode					
Shutdown	-	-	2.0	-	µA

5.8 WLAN RF Characteristics - Receiver

Measured with T = 25 ℃, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b	1 Mbps DSSS	-	-99	-	dBm
	2 Mbps DSSS	-	-95	-	dBm
	5.5 Mbps DSSS	-	-93	-	dBm
	11 Mbps DSSS	-	-89	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-87	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-81	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HT20, MCS0	-	-93	-	dBm
	HT20, MCS1	-	-92	-	dBm
	HT20, MCS2	-	-89	-	dBm
	HT20, MCS3	-	-87	-	dBm
	HT20, MCS4	-	-83	-	dBm
	HT20, MCS5	-	-79	-	dBm
	HT20, MCS6	-	-77	-	dBm
	HT20, MCS7	-	-75	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz	HT40, MCS0	-	TBD	-	dBm
	HT40, MCS1	-	TBD	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER for 4096 octet PSDU, LDPC)	HT40, MCS2		-	TBD	-	dBm
	HT40, MCS3		-	TBD	-	dBm
	HT40, MCS4		-	TBD	-	dBm
	HT40, MCS5		-	TBD	-	dBm
	HT40, MCS6		-	TBD	-	dBm
	HT40, MCS7		-	TBD	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HE20, MCS0		-	-92	-	dBm
	HE20, MCS1		-	-91	-	dBm
	HE20, MCS2		-	-88	-	dBm
	HE20, MCS3		-	-86	-	dBm
	HE20, MCS4		-	-82	-	dBm
	HE20, MCS5		-	-78	-	dBm
	HE20, MCS6		-	-76	-	dBm
	HE20, MCS7		-	-74	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	TBD	-	dBm
	11g: 6 ~54 Mbps (10% PER, 1024 octets)		-	10	-	dBm
	11n: MCS0~7 (10% PER, 4096 octets)		-	10	-	dBm
	11ax: MCS0~7 (10% PER, 4096 octets)		-	TBD	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	TBD	-	dB
	2 Mbps DSSS	-74 dBm	-	TBD	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	TBD	-	dB
	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1024 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	TBD	-	dB
	54 Mbps OFDM	-62 dBm	-	26	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	-	TBD	-	dB
	HT20, MCS7	-61 dBm	-	25	-	dB
	HT40, MCS0	TBD	-	TBD	-	dB
	HT40, MCS7	TBD	-	TBD	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE20, MCS0	TBD	-	TBD	-	dB
	HE20, MCS7	TBD	-	TBD	-	dB
General Spurs						
General spurs	1~18 GHz		-	TBD	-	dBm

5.9 WLAN RF Characteristics - Transmitter

Measured with T = 25 ℃, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX Power					
TX power - IEEE 802.11b	1 Mbps DSSS	-	18	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
(EVM compliant)	11 Mbps DSSS		-	18	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM		-	17	-	dBm
	54 Mbps OFDM		-	16	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0		-	17	-	dBm
	HT20, MCS7		-	15	-	dBm
	HT40, MCS0		-	TBD	-	dBm
	HT40, MCS7		-	TBD	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0		-	TBD	-	dBm
	HE20, MCS7		-	TBD	-	dBm
Harmonic Level						
Harmonic level (at maximum output power)	4.8~5.0 GHz	2nd harmonic	-	TBD	-	dBm
	7.2~7.5 GHz	3rd harmonic	-	TBD	-	dBm
General Spurs						
General spurs (at maximum output power)	1~18 GHz		-	TBD	-	dBm

5.10 Bluetooth LE RF Characteristics - Receiver

Measured with T = 25 ℃, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Data rate	Bluetooth LE 1 Mbps, 2 Mbps, 125 kbps and 500 kbps				
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-97	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB
C/I 1 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -1 MHz adjacent to image channel	-	-	TBD	-	dB
Out-of-band blocking	30-2000 MHz	-10	-	-	dBm
Out-of-band blocking	2003-2399 MHz	-20	-	-	dBm
Out-of-band blocking	2484-2997 MHz	-10	-	-	dBm
Out-of-band blocking	3000 MHz-12.75 GHz	-10	-	-	dBm
Intermodulation	P_{IN} = -64 dBm; f0 = 2f1 - f2, f2 - f1 = 3 MHz or 4 MHz or 5 MHz	-	-	-23	dBm
Leakage @ < 1 GHz	-	-	TBD	-	dBm
Leakage @ > 1 GHz	-	-	TBD	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 4 MHz adjacent channel	-	-	TBD	-	dB
C/I -4 MHz adjacent channel	-	-	TBD	-	dB
C/I 6 MHz adjacent channel	-	-	TBD	-	dB
C/I -6 MHz adjacent channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I > 6 MHz adjacent channel	-	-	TBD	-	dB
C/I < -6 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB
C/I 2 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -2 MHz adjacent to image channel	-	-	TBD	-	dB
Out-of-band blocking	30-2000 MHz	TBD	-	-	dBm
Out-of-band blocking	2003-2399 MHz	TBD	-	-	dBm
Out-of-band blocking	2484-2997 MHz	TBD	-	-	dBm
Out-of-band blocking	3000 MHz-12.75 GHz	TBD	-	-	dBm
Intermodulation	P_{IN} = -64 dBm; dBm; f0 = 2f1 - f2, f2 - f1 = 3 MHz or 4 MHz or 5 MHz	-	-	TBD	dBm
Leakage @ < 1 GHz	-	-	TBD	-	dBm
Leakage @ > 1 GHz	-	-	TBD	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 1 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -1 MHz adjacent to image channel	-	-	TBD	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB
C/I image channel	-	-	TBD	-	dB
C/I 1 MHz adjacent to image channel	-	-	TBD	-	dB
C/I -1 MHz adjacent to image channel	-	-	TBD	-	dB

5.11 Bluetooth LE RF Characteristics - Transmitter

Measured with T = 25 ℃, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
TX Power					
TX power	-	-20	5	15	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps					
In-band Emissions					
±2 MHz offset	-	-	TBD	-	dBm
±3 MHz offset	-	-	TBD	-	dBm
> ±3 MHz offset	-	-	TBD	-	dBm
Modulation Characteristics					
Δf1avg	-	-	TBD	-	kHz
Δf2max	-	-	TBD	-	kHz
Δf2avg/Δf1avg	-	-	TBD	-	-
Carrier Frequency Offset and Drift					
Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	TBD	-	kHz
$\|f_1 - f_0\|$	-	-	TBD	-	kHz
Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	TBD	-	kHz/50 μs
Bluetooth LE 2 Mbps					
In-band Emissions					
±4 MHz offset	-	-	TBD	-	dBm
±5 MHz offset	-	-	TBD	-	dBm
> ±5 MHz offset	-	-	TBD	-	dBm
Modulation Characteristics					
Δf1avg	-	-	TBD	-	kHz
Δf2max	-	-	TBD	-	kHz
Δf2avg/Δf1avg	-	-	TBD	-	-
Carrier Frequency Offset and Drift					
Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	TBD	-	kHz
$\|f_1 - f_0\|$	-	-	TBD	-	kHz

Parameter	Condition	Min.	Typ.	Max.	Unit
Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	TBD	-	kHz/50 μs
Bluetooth LE 125 kbps					
In-band Emissions					
±2 MHz offset	-	-	TBD	-	dBm
±3 MHz offset	-	-	TBD	-	dBm
> ±3 MHz offset	-	-	TBD	-	dBm
Modulation Characteristics					
Δf1avg	-	-	TBD	-	kHz
Δf1max	-	-	TBD	-	kHz
Carrier Frequency Offset and Drift					
Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	TBD	-	kHz
$\|f_0 - f_3\|$	-	-	TBD	-	kHz
$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	TBD	-	kHz/48 μs
Bluetooth LE 500 kbps					
In-band Emissions					
±2 MHz offset	-	-	TBD	-	dBm
±3 MHz offset	-	-	TBD	-	dBm
> ±3 MHz offset	-	-	TBD	-	dBm
Modulation Characteristics					
Δf2avg	-	-	TBD	-	kHz
Δf2max	-	-	TBD	-	kHz
Carrier Frequency Offset and Drift					
Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	-	kHz
Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	TBD	-	kHz
$\|f_0 - f_3\|$	-	-	TBD	-	kHz
$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	TBD	-	kHz/48 μs

5.12 SAR ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	-	-	26	MHz
Conversion time	-	-	16	-	Cycle
VREF	Internal	-	1.2	-	V
	External	-	VIO/2	-	V
No missing code	-	-	TBD	-	Bit
Input voltage range	-	0	-	VREF*2	V
Input impedance	-	10	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-2	-	2	LSB
INL	-	-2	-	2	LSB
ENOB	-	-	TBD	-	Bit
Offset temperature drift	-	-	TBD	-	LSB/℃
Gain temperature drift	-	-	TBD	-	%/℃
SNDR	-	-	TBD	-	dB
SFDR	-	-	TBD	-	dB
$T_{STARTUP}$	-	-	TBD	-	μs
Current consumption	With buffer	-	TBD	-	μA

6. Package Information

6.1 QFN80 8 x 8 mm Package

Figure 6-1 QFN80 8 x 8 mm Package Outline

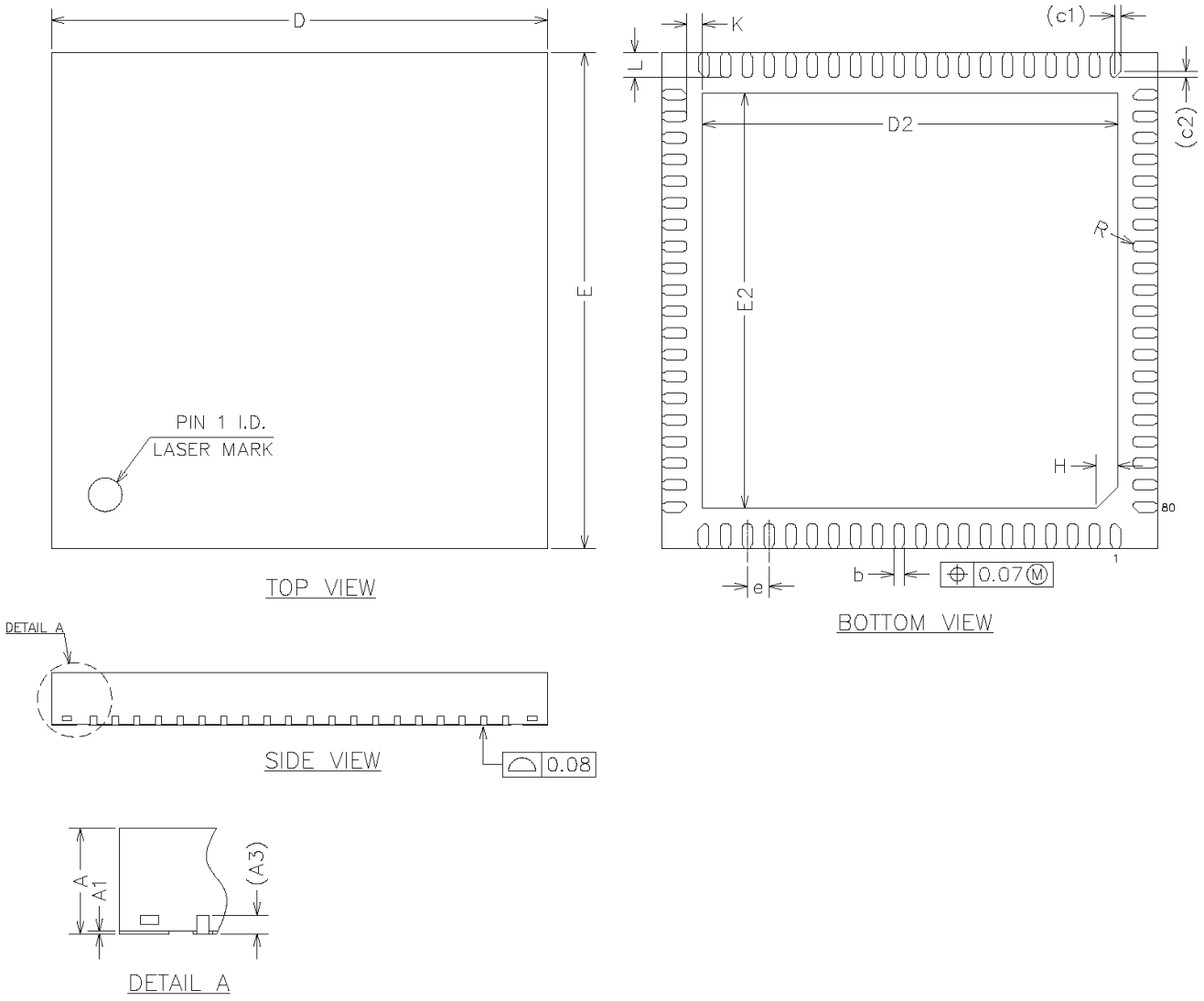


Table 6-1 QFN80 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.12	0.17	0.22
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.60	6.70	6.80
E2	6.60	6.70	6.80
e	0.35 BSC		
H	0.35 REF		
K	0.15	0.25	0.35
L	0.30	0.40	0.50
R	0.065	-	-
c1	-	0.10	-
c2	-	0.10	-

6.2 QFN68 8 x 8 mm Package

Figure 6-2 QFN68 8 x 8 mm Package Outline

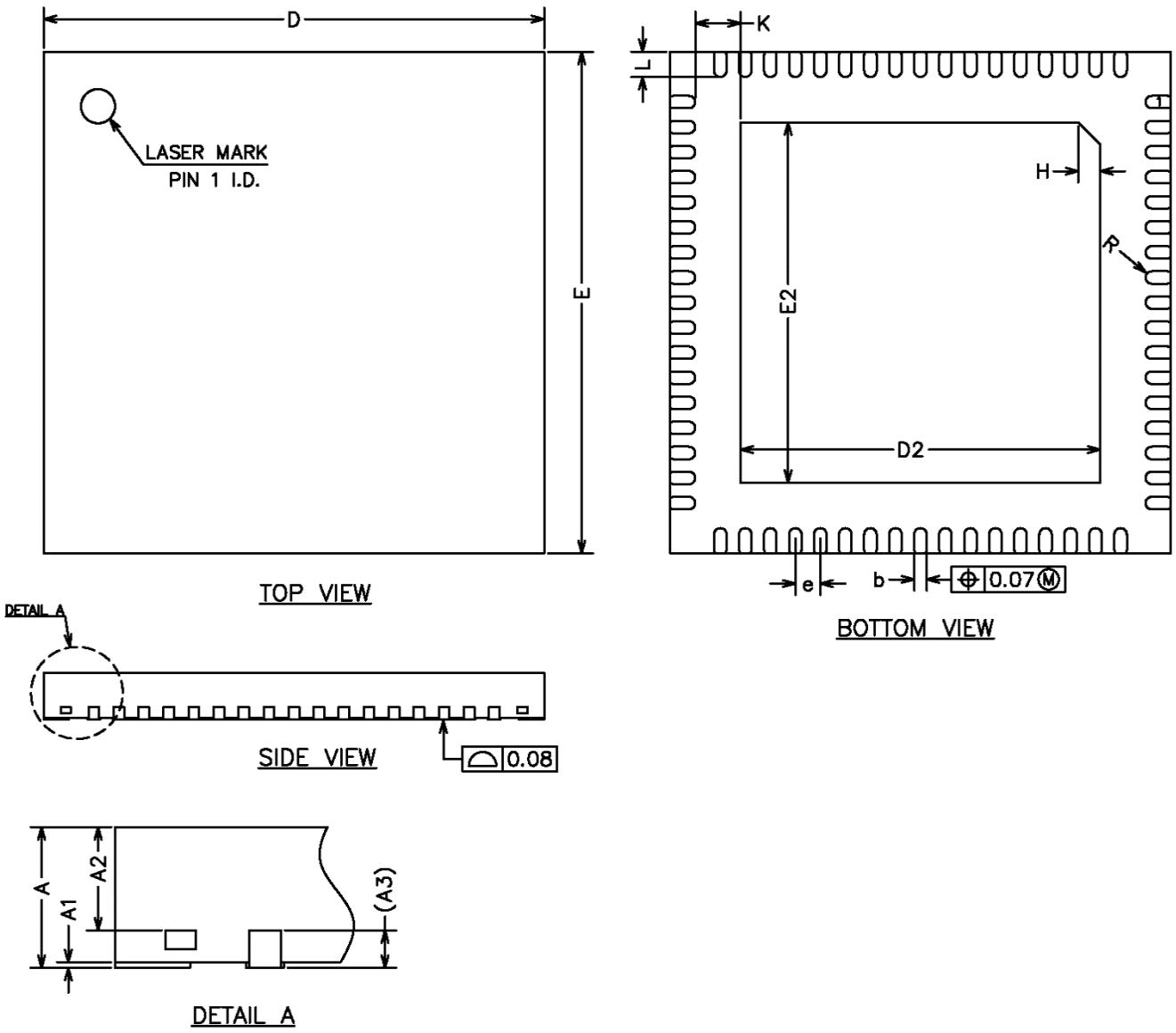


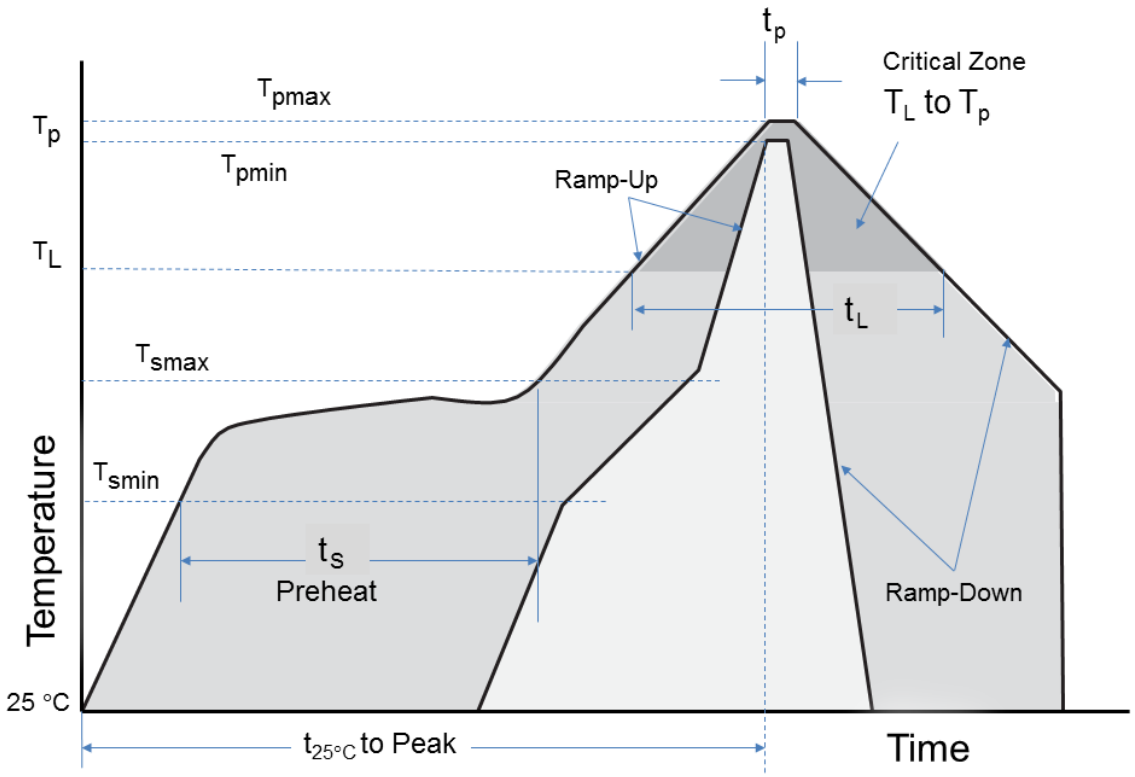
Table 6-2 QFN68 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.65	5.75	5.85
E2	5.65	5.75	5.85
e	0.30	0.40	0.50
H	0.35 REF		
K	0.625	-	-
L	0.30	0.40	0.50
R	0.09	-	-

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 ℃/s max.

Profile Feature	Specification
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Part Number Scheme

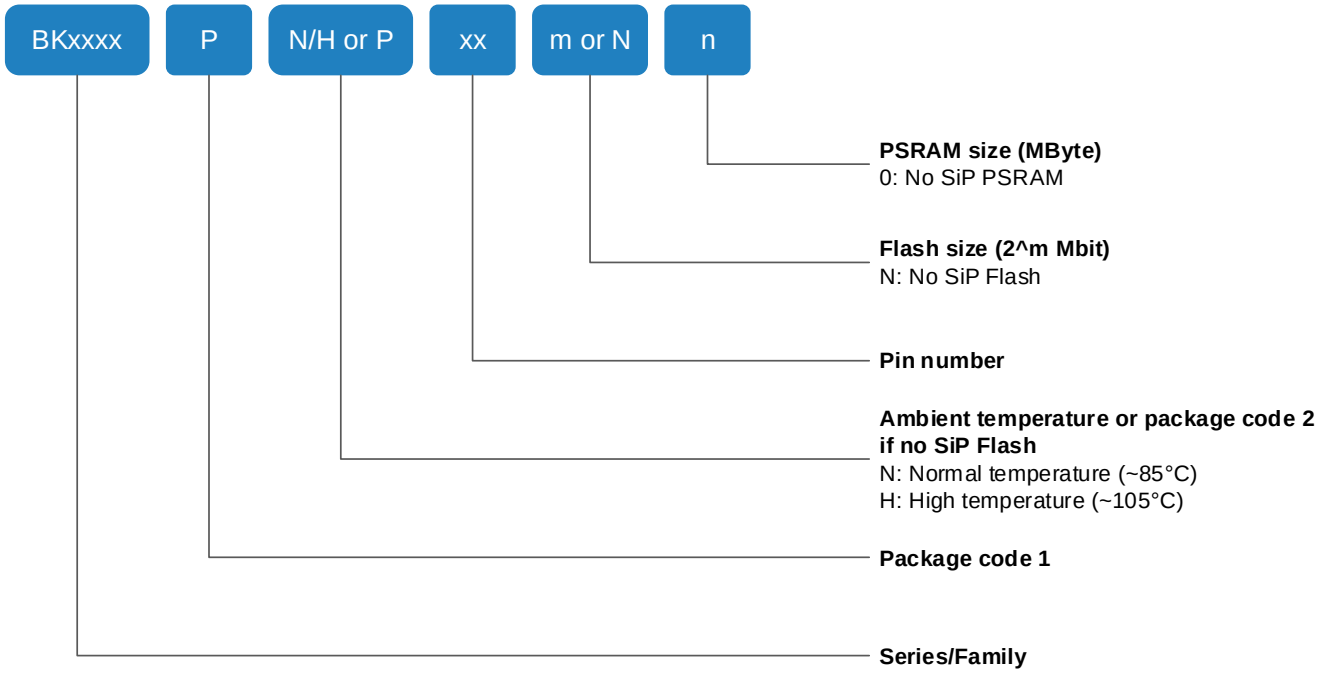


Table 8-1 Ordering Information

Ordering Code	Package	SiP[a] Flash	SiP PSRAM	Packing	Minimum Ordering Qty (MOQ)
BK7256QN80N8	8 mm x 8 mm QFN80	-	8 MB	Tape and Reel	3000
BK7256QN6858	8 mm x 8 mm QFN68	4 MB	8 MB	Tape and Reel	3000

a. A system in a package (SiP) refers to Flash/PSRAM enclosed in the package.

Revision History

Version	Date	Description
0.1	2022/2/28	Initial release. First version of the preliminary specification.
1.0	2022/11/21	• General wording fixes • Added documentation for QFN80 package • Updated secure element description and added KDF in subsection Security under Section 1 Features • Corrected the channel number of GDMA • Listed applications in Section 1 Features • Removed TRNG from Figure 2-1 in Section 2 Overview • Inverted pin assignment for UART CTS and RTS signals in Section 3 Pin Description • Updated the description for general-purpose timers, watchdogs, and RTC • Added GPIO mapping for RGB888 interface to Table 4-2 in Section 4.17 LCD • Changed Section Security into Section 4.30 Secure Element • Updated RF characteristics tables in Section 5.8 to Section 5.11

Copyright

Disclaimer

The documentation is provided on an "as-is" basis only. Beken reserves the right to make any updates, corrections and any other modifications to its documentation without further notice and limitation to product information, descriptions, and specifications herein. Beken does not give warranties as to the accuracy or completeness of the included information. Beken shall have no liability for any use of the information in this documentation. You should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Information published by Beken regarding any third-party products does not constitute a license to use such products or a warranty or endorsement thereof. Use of such information may require a license from a third party under the intellectual property rights of such third party, or a license from Beken under the intellectual property rights of Beken.

Trademarks

Beken, the BEKEN logo and combinations thereof are trademarks or registered trademarks of Beken. All other product or brand names mentioned herein are trademarks or registered trademarks of their respective holders.

Beken Corporation

Building 41, 1387 Zhangdong Rd

Shanghai 201203

China

http://www.bekencorp.com